

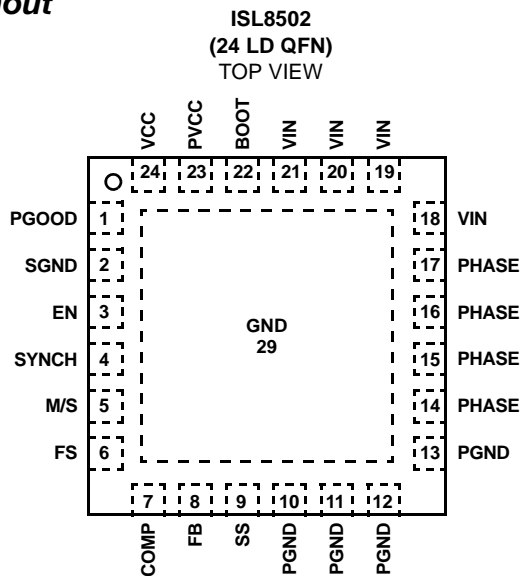
The ISL8502 is a synchronous buck controller with internal MOSFETs packaged in a small 4mmx4mm QFN package. The ISL8502 can support a continuous load of 2A and has a very wide input voltage range. With the switching MOSFETs integrated into the IC, the complete regulator footprint can be very small and provide a much more efficient solution than a linear regulator.

The ISL8502 is capable of standalone operation or it can be used in a master slave combination for multiple outputs that are derived from the same input rail. Multiple slave channels can be individually programmed such that the internal clocks are out-of-phase. This method minimizes the ripple on the input rail.

The switching PWM controller drives two internal N-Channel MOSFETs in a synchronous-rectified buck converter topology. The synchronous buck converter uses voltage-mode control with fast transient response. The switching regulator provides a maximum static regulation tolerance of $\pm 1\%$ over line, load, and temperature ranges. The output is user-adjustable by means of external resistors down to 0.6V.

The output is monitored for undervoltage events. The switching regulator also has over current protection. Thermal shutdown is integrated. The ISL8502 features a bidirectional Enable pin that allows the part to shut itself down and pull the enable pin low at the same time.

Pinout



Features

- 2A Continuous Output Current
- Integrated MOSFETs for Small Regulator Footprint
- Adjustable Switching Frequency, 500kHz to 1.2MHz
- Tight Output Voltage Regulation, $\pm 1\%$ Over-Temperature
- Wide Input Voltage Range, 5V $\pm 10\%$ or 5.5V to 14V
- Wide Output Voltage Range, from 0.6V
- Simple Single-Loop Voltage-Mode PWM Control Design
- Input Voltage Feed-Forward for Constant Modulator Gain
- Fast PWM Converter Transient Response
- Lossless $r_{DS(ON)}$ High Side and Low Side Overcurrent Protection
- Undervoltage Detection
- Integrated Thermal Shutdown Protection
- Power-Good Indication
- Adjustable Soft-Start
- QFN Package
 - Compliant to JEDEC PUB95 MO-220 QFN (Quad Flat No Leads) package outline
 - Near Chip Scale Package footprint, which improves PCB efficiency and has a thinner profile
- Pb-Free (RoHS Compliant)

Applications

- Point of Load Applications
- Graphics Cards - GPU and Memory Supplies
- ASIC Power Supplies
- Embedded Processor and I/O Supplies
- DSP Supplies

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL8502IRZ*	85 02IRZ	-40 to +85	24 Ld 4x4 QFN	L24.4x4D

*Add "-T" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

What's Inside

The Evaluation Board Kit contains the following materials:

- The ISL8502 EVAL REVD board
- The ISL8502 datasheet
- This EVAL KIT document

Recommended Equipment

The following materials are recommended to perform testing:

- 0V to 15V power supply with at least 5A source current capability, battery, notebook AC adapter
- Two Electronic Loads capable of sinking current up to 5A
- Digital Multimeters (DMMs)
- 100MHz quad-trace Oscilloscope
- Signal generator (only if the SYNC function needs to be evaluated)

Quick Setup Guide

1. Ensure that the circuit is correctly connected to the supply and loads prior to applying any power.
2. Connect the bias supply to VIN. Plus terminal to J1(VIN) and negative return to J2(GND).
3. Verify that all positions are ON for S1, EN_all, EN_1, EN_2.
4. Turn on the power supply.
5. Verify the outputs voltages are 2.5V for V_{OUT1} and V_{OUT2}.

Evaluating Other Output Voltages

The ISL8502EVAL kit outputs are preset to 2.5V. For a quick evaluation of output voltages between 0.6V and V_{IN} - 1.7V, the following resistors need to be changed in the feedback network as shown in Equations 1 and 2:

$$R_{111} = (R_{108}) / [(V_{OUT} / V_{FB1}) - 1] \quad (\text{EQ. 1})$$

where R₁₀₈ = 17.4kΩ; and V_{FB1} = 0.6V

$$R_{211} = (R_{208}) / [(V_{OUT2} / V_{FB2}) - 1] \quad (\text{EQ. 2})$$

where R₂₀₈ = 17.4kΩ; and V_{FB2} = 0.6V

However, for reliable operation over the entire load and temperature range, it is highly recommended to follow the output filter and loop compensation network design guidelines as listed in the ISL8502 datasheet.

<http://www.intersil.com/data/fn/fn6389.pdf>

Frequency

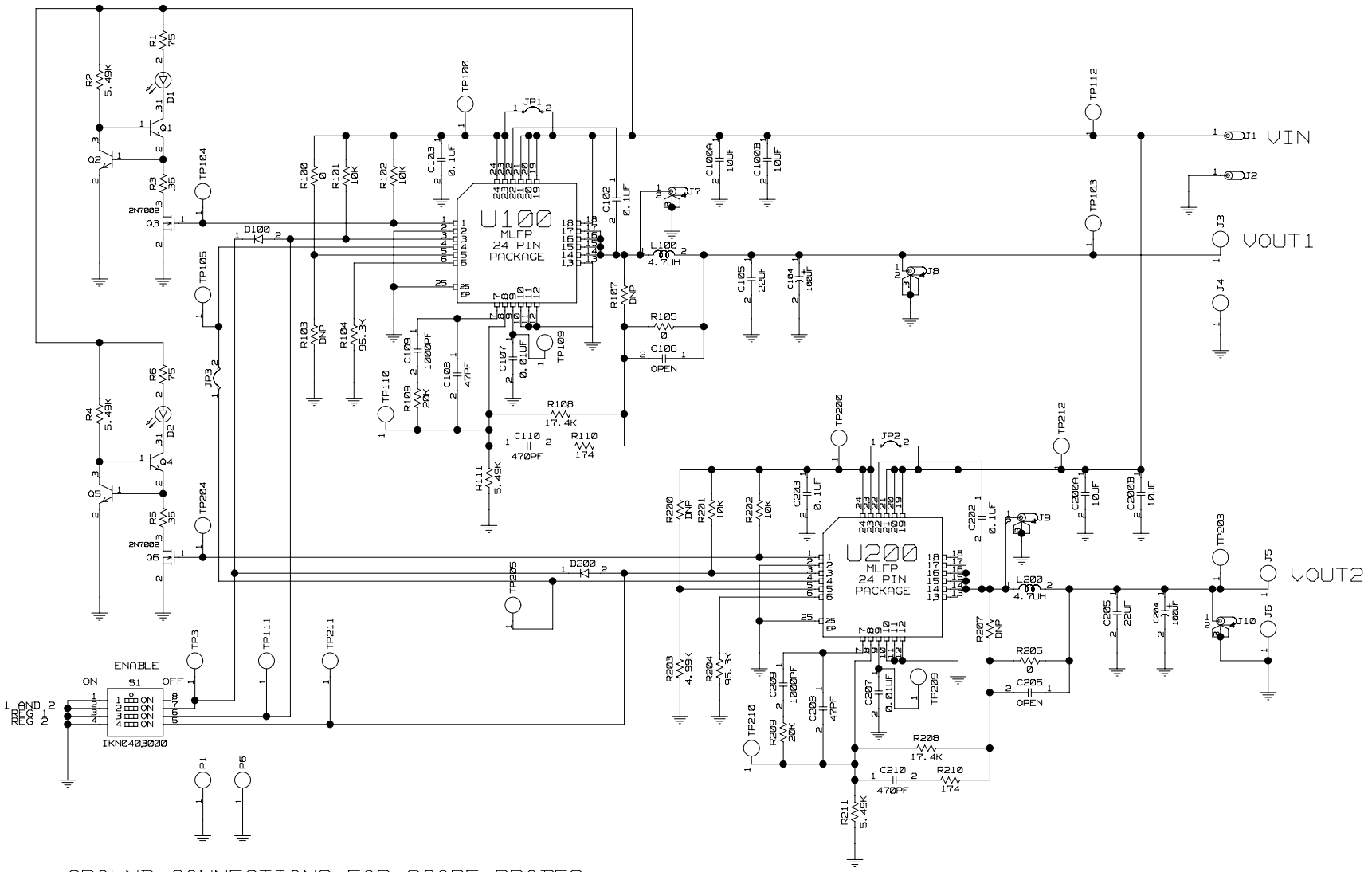
The ISL8502EVAL can operate at switching frequencies from 500kHz to 1.2MHz. R₁₀₄ and R₂₀₄ are used to program the switching frequency through Equation 3:

$$R_{104} \text{ and } (R_{204}) = 48000 / (f_{osc}[\text{kHz}]) \quad (\text{EQ. 3})$$

TABLE 1. SWITCH 1 SETTINGS

SW1	SKIP	OPERATING MODE
1	NC	No Connect
2	EN_ALL	Enable or disable V _{OUT1} and V _{OUT2}
3	EN1	Enable or disable V _{OUT1}
4	EN2	Enable or disable V _{OUT2}

ISL8502EVAL1Z Schematic



GROUND CONNECTIONS FOR SCOPE PROBES

Application Note 1277

TABLE 2. COMPONENT LIST

REF DES	QTY	VALUE	TOL.	VOLTAGE	PACKAGE	PART NUMBER	MANUFACTURER	DESCRIPTION
C100A, C100B, C200A, C200B	4	10 μ F	20%	25V	SM1206	-	AVX, Samsung, TDK, Murata	Multilayer Capacitor
C102, C202	2	0.1 μ F	10%	16V	SM0402	-	AVX, Samsung, TDK, Murata	Multilayer Capacitor
C103, C203	2	1 μ F	20%	6.3V	SM0402	-	AVX, Samsung, TDK, Murata	Multilayer Capacitor
C104, C204	2	100 μ F	20%	35V	RADIAL	-	SANYO	Radial Elect. MV_AX Series Cap
C105, C205	2	22 μ F	20%	10V	SM0402	-	AVX, Samsung, TDK, Murata	Multilayer Capacitor
C106, C206	2	OPEN	-	-	SM0402	-	AVX, Samsung, TDK, Murata	Multilayer Capacitor
C107, C207	2	0.1 μ F	10%	16V	SM0402	-	AVX, Samsung, TDK, Murata	Multilayer Capacitor
C108, C208	2	47pF	5%	50V	SM0402	-	AVX, Samsung, TDK, Murata	Multilayer Capacitor
C109, C209	2	1000pF	10%	50V	SM0402	-	AVX, Samsung, TDK, Murata	Multilayer Capacitor
C110, C210	2	470pF	10%	50V	SM0402	-	AVX, Samsung, TDK, Murata	Multilayer Capacitor
D1, D2	2	-	-	-	-	LTST-C170CKT	LITEON	AlGaAs on GaAs Red LED
D100, D200	2	-	-	-	-	IN4148WS	DIODES	Fast Switching Diode
J1, J2	2	-	-	-	-	111-0701-001	JOHNSON-COMP	Binding Post White
J3-J6, P1, P6	6	-	-	-	-	PAD_150	GENERIC	0.150Pad with 0.110 Plated Thru Hole
JP1-JP3	3	-	-	-	-	JUMPER2_100	GENERIC	Two Pin Jumper
L100, L200	2	4.7 μ H	-	19m Ω	6_3X8_3	CDRH8D28-4R7	SUMIDA	SMT Power Inductor
Q1, Q2, Q4, Q5	4	-	-	30V	SOT23	MMBT2222LT1	MOTOROLA	NPN Transistor
Q3, Q6	2	-	-	60V	SOT23	2N7002	FAIRCHILD	N-Channel EMF Effect Transistor
R1, R6	2	75	5%	100V	SM0402	-	Generic	Thick Film Chip Resistor
R100, R105, R205	3	0	1%	100V	SM0402	-	Generic	Thick Film Chip Resistor
R101, R102, R201, R202	4	10k	1%	100V	SM0402	-	Generic	Thick Film Chip Resistor
R103, R107, R200, R207	4	DNP	1%	100V	SM0402	-	Generic	Thick Film Chip Resistor
R104, R204	2	95.3k	1%	100V	SM0402	-	Generic	Thick Film Chip Resistor
R108, R208	2	17.4k	1%	100V	SM0402	-	Generic	Thick Film Chip Resistor
R109, R209	2	20k	1%	100V	SM0402	-	Generic	Thick Film Chip Resistor
R110, R210	2	174	1%	100V	SM0402	-	Generic	Thick Film Chip Resistor
R2, R4, R111, R211	4	5.49k	1%	100V	SM0402	-	Generic	Thick Film Chip Resistor
R203	1	4.99k	1%	100V	SM0402	-	Generic	Thick Film Chip Resistor

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TABLE 2. COMPONENT LIST (Continued)

REF DES	QTY	VALUE	TOL.	VOLTAGE	PACKAGE	PART NUMBER	MANUFACTURER	DESCRIPTION
R3, R5	2	36	5%	100V	SM0402	-	Generic	Thick Film Chip Resistor
S1	1	-	-	-	-	IKN0403000	APEM	IK Series High Rel SPST SMT DIP Switch
TP3, TP100, TP103-TP105, TP109-TP112, TP200, TP203-TP205, TP209-TP212	17	-	-	-	-	PAD_75	Generic	0.075 Pad with 0.036 Plated Thru Hole
U100, U200	2	-	-	-	QFN	ISL8502	Intersil	Synchronous Buck Regulator

ISL8502EVAL1Z Board Layout

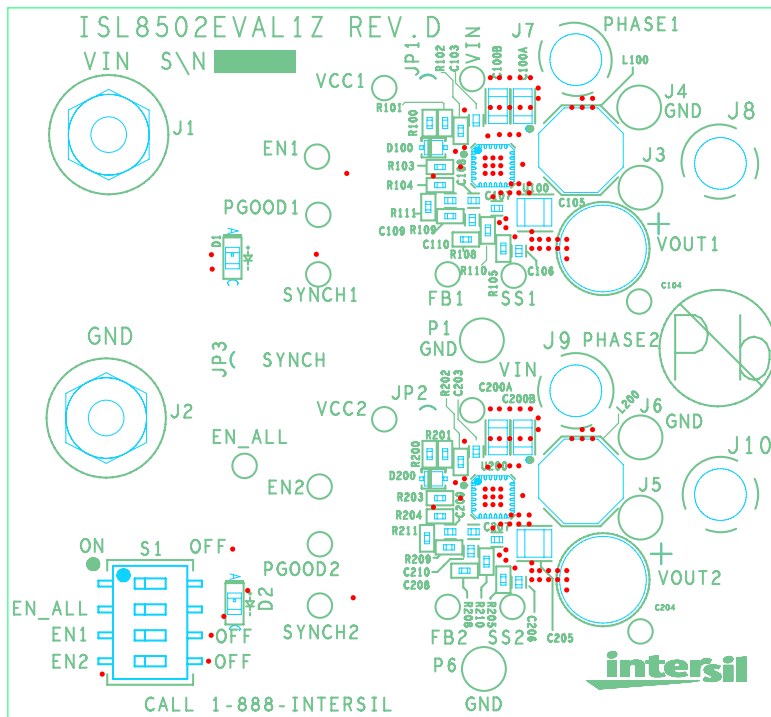


FIGURE 1. TOP COMPONENTS

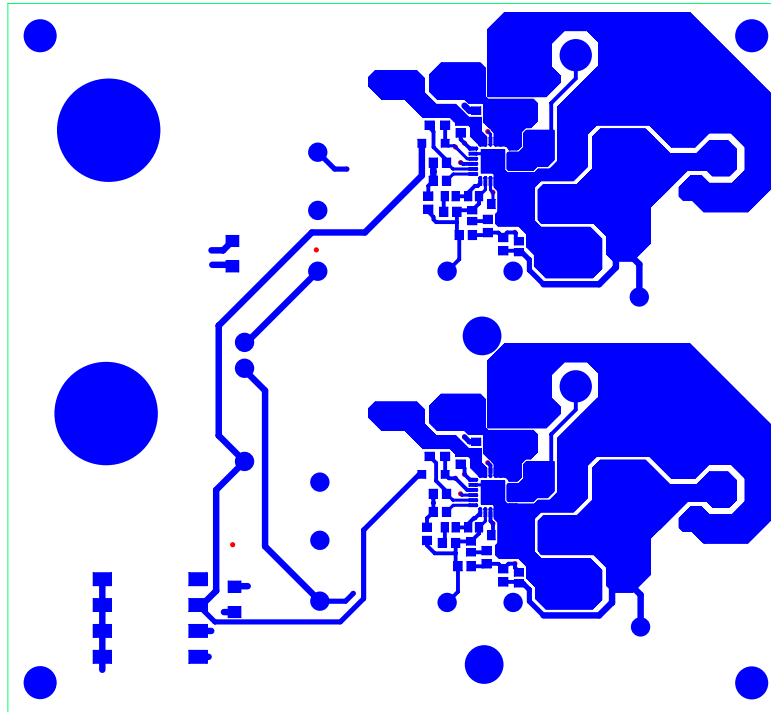


FIGURE 2. TOP LAYER ETCH

ISL8502EVAL1Z Board Layout (Continued)

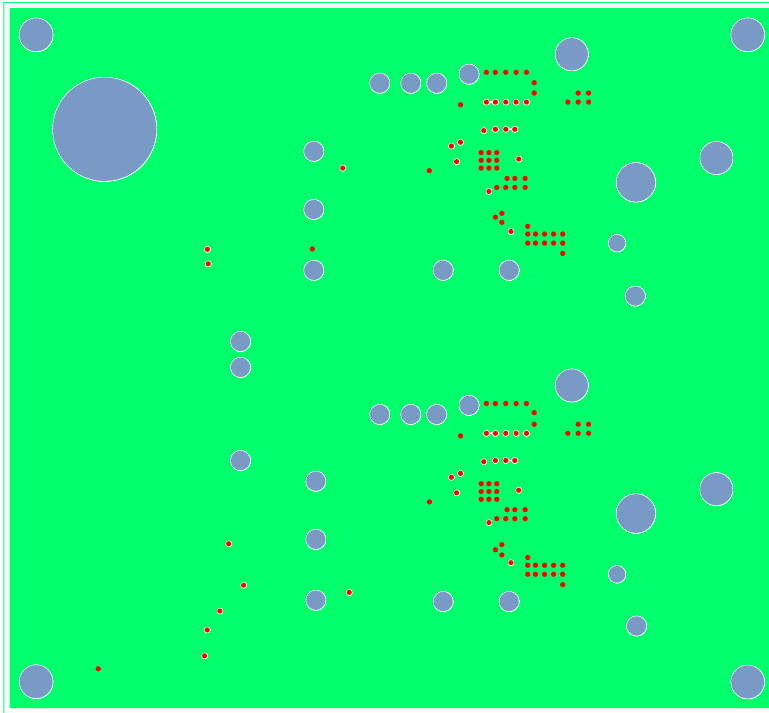


FIGURE 3. 2ND LAYER ETCH

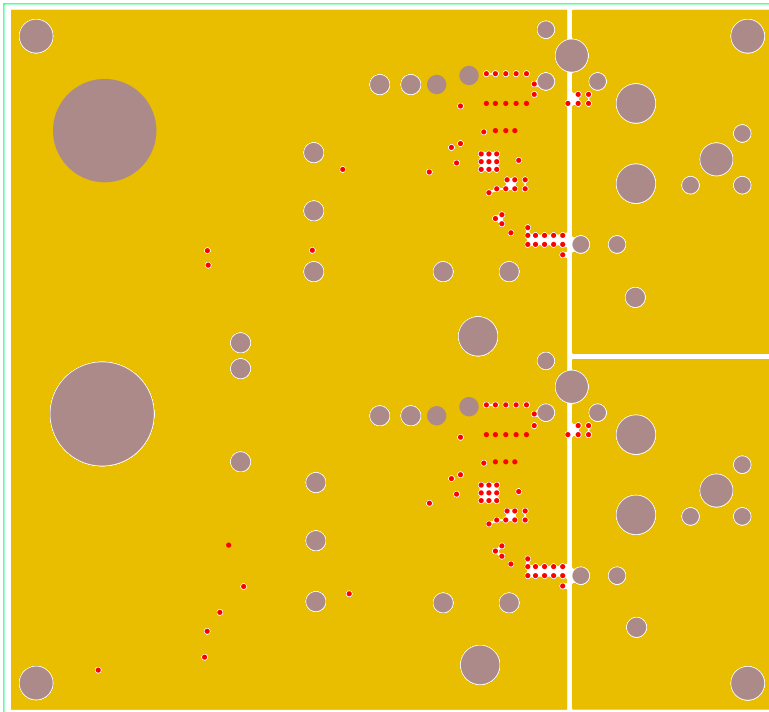


FIGURE 4. 3RD LAYER ETCH

ISL8502EVAL1Z Board Layout (Continued)

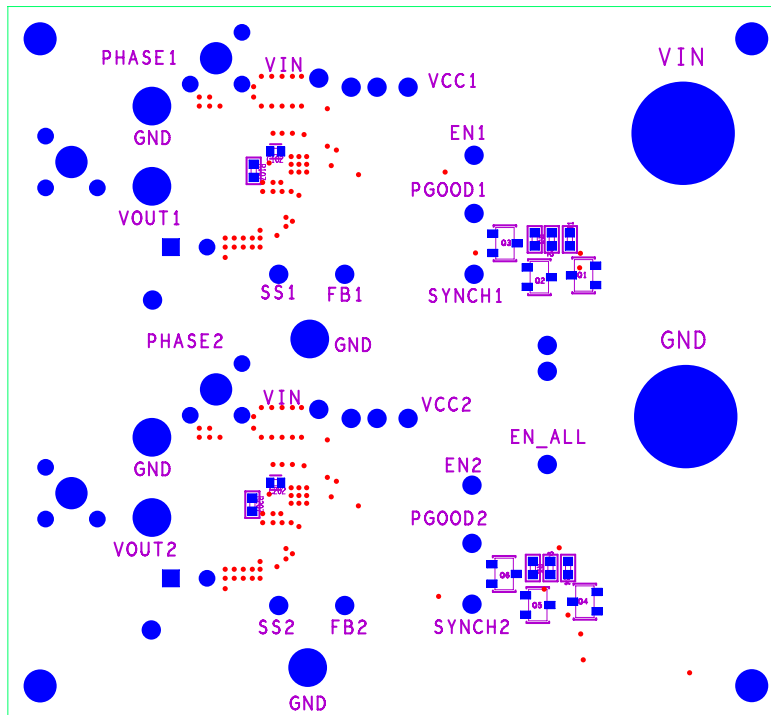


FIGURE 5. BOTTOM LAYER COMPONENTS (MIRRORED)

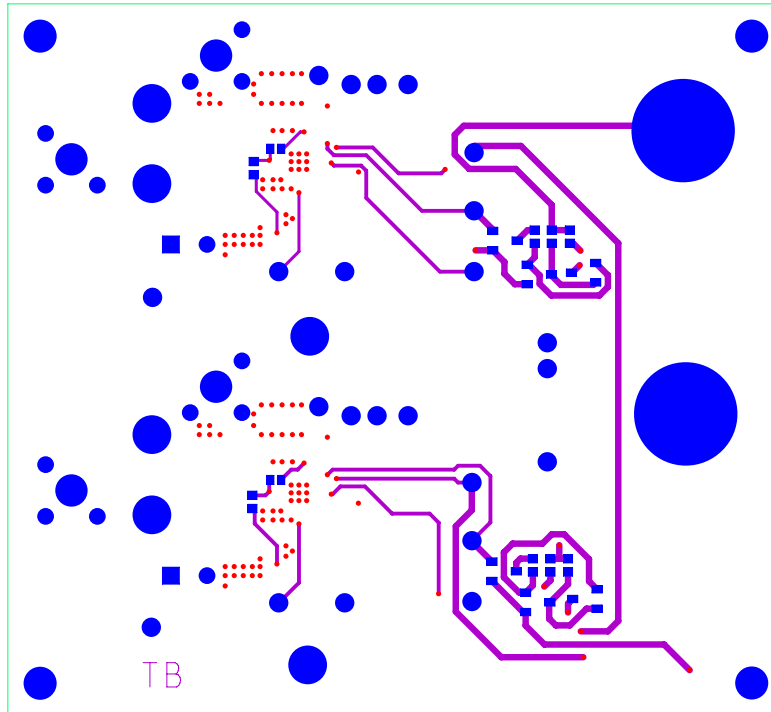


FIGURE 6. BOTTOM LAYER ETCH (MIRRORED)

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